VHDL

```
library ieee;
use ieee.std_logic_1164.all;
-------------------------------------------------

entity AND_Gate is
port(  x: in std_logic;
       y: in std_logic;
       F: out std_logic
);
end AND_ent;

-------------------------------------------------

architecture AND_arch of AND_Gate is
begin

F <= x AND y;

end AND_arch;

-------------------------------------------------
```

Verilog

```
module some_logic_component (c, a, b);
      // declare port signals
 output c;
 input a, b;
     // declare internal wire
 wire d;
     //instantiate structural logic gates
 and a1(d, a, b); //d is output, a and b are inputs
 not n1(c, d);    //c is output, d is input
endmodule
```