IR2110

HIGH AND LOW SIDE DRIVER

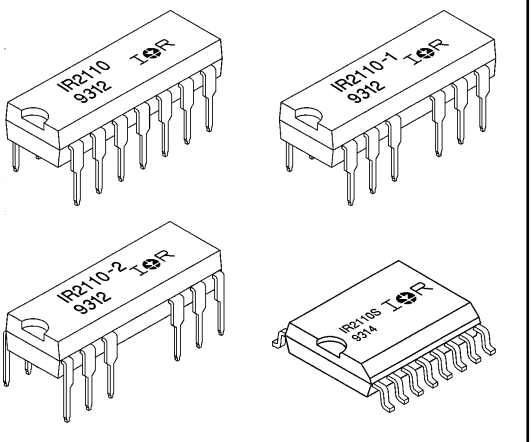
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	500V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

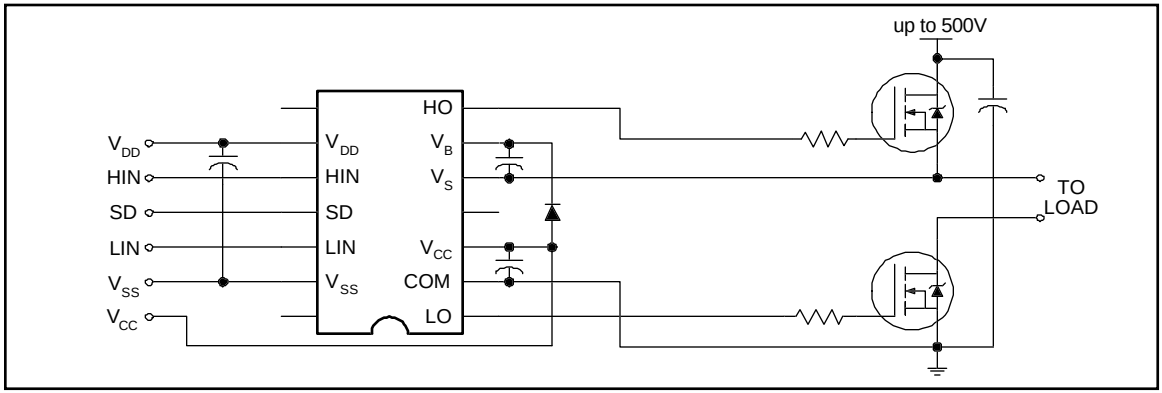
Packages



Description

The IR2110 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 volts.

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	525	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	—	1.6	
	(16 Lead SOIC)	—	1.25	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 5 & 6)	—	75	
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	500	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 5	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

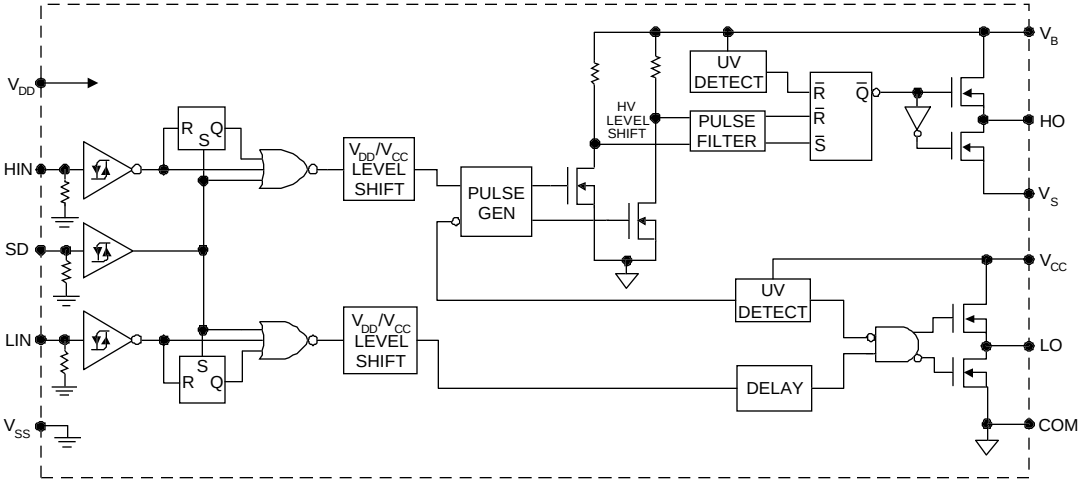
Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	8	—	94	125		V_S = 500V
t_{sd}	Shutdown Propagation Delay	9	—	110	140		V_S = 500V
t_r	Turn-On Rise Time	10	—	25	35		
t_f	Turn-Off Fall Time	11	—	17	25		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	10		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset Supply Leakage Current	16	—	—	50	µA	V_B = V_S = 500V
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.0	8.2	9.4		
I_{O+}	Output High Short Circuit Pulsed Current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

Functional Block Diagram



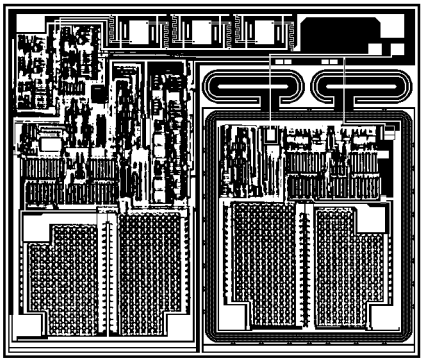
Lead Definitions

Lead Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

14 Lead DIP	14 Lead DIP w/o Lead 4	16 Lead DIP w/o Leads 4 & 5	16 Lead SOIC (Wide Body)
IR2110	**IR2110-1**	**IR2110-2**	**IR2110S**
Part Number			

Device Information

Process & Design Rule		HVDCMOS 4.0 µm
Transistor Count		220
Die Size		100 X 117 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
First Layer	Width	4 µm
	Spacing	6 µm
	Thickness	5000Å
	Material	Al - Si (Si: 1.0% ±0.1%)
Second Layer	Width	6 µm
	Spacing	9 µm
	Thickness	20,000Å
Contact Hole Dimension		8 µm X 8 µm
Insulation Layer	Material	PSG (SiO_2)
	Thickness	1.5 µm
Passivation (1)	Material	PSG (SiO_2)
	Thickness	1.5 µm
Passivation (2)	Material	Proprietary*
	Thickness	Proprietary*
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	14 & 16 Lead PDIP / 16 Lead SOIC
	Materials	EME6300 / MP150 / MP190
Remarks: * Patent Pending		

Harris Semiconductor

APPNOTE

No. AN9010.4 April 1994

Harris Intelligent Power

HIP2500 HIGH VOLTAGE ($500V_{DC}$) HALF-BRIDGE DRIVER IC

Author: George E. Danz

Introduction

The HIP2500 is an high voltage, high speed half-bridge driver for driving n-channel MOS gated power devices. The blocking voltage of the HIP2500 is 500VDC which provides the capability for application on most rectified 230VAC line. The HIP2500 uses the same proprietary technology which resulted in the first products in the HVIC (high voltage IC) family, the SP600/SP601 Half-Bridge Drivers.

The upper and lower drivers are junction-isolated from each other and controlled by independent input lines referenced to the system common. The HIP2500 offers a reliable, cost-effective means for driving high-side referenced n-channel power switches from ground referenced logic. Level-translation circuitry using optocouplers or, the more reliable, but often too expensive, transformer is not required. Highly integrated logic and drive circuitry minimizes propagation delays and allows higher switching frequencies and lower switching losses than would be attainable using more conventional techniques. Besides cost savings and performance increases, the HIP2500 simplifies and reduces the effort needed to design efficient MOS gated high and low side switch drivers.

The HIP2500 boasts high output drive capability (2A peak), while still employing the PMOS source and NMOS sink drivers which are also employed in the SP600 family. By removing the Overcurrent trip, automatic refresh and shoot-through protection features of the SP600 family, the simpler logic circuitry allows lower transport delays from input to output and operation at PWM frequencies as high as 500KHz. Gate rise and fall times are as low as 20ns into a 1000pF load.

While the burden of shoot-through protection now rests squarely with the user, the simplicity of precise user gate control allows the capability to drive double forward converters, a configuration popularly used in power supply, stepper motor and switched reluctance motor controls. Capacitor C_F, referred to as the “bootstrap capacitor,” must always be fully pre-charged before turning on the upper switch. On power up, therefore, the lower switch should be turned on first, providing a charging path for C_F from V_{CC} through the bootstrap diode D_F and back to ground. Figure 1 and Figure 2 both show the bootstrap components.

An inductive load will often supply the current required to charge the bootstrap capacitor each time the upper switch is turned off. It does this through a lower flyback diode as shown in Figure 2, or the internal body diode of a lower MOSFET as shown in Figure 4**.** In the case of the buck converter, the load provides a path to pre-charge the bootstrap capacitor prior to turning on the high side switch.

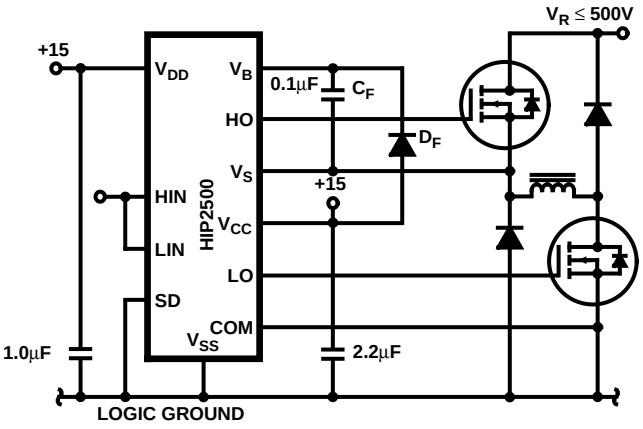


FIGURE 1. DOUBLE FORWARD CONVERTER SCHEMATIC

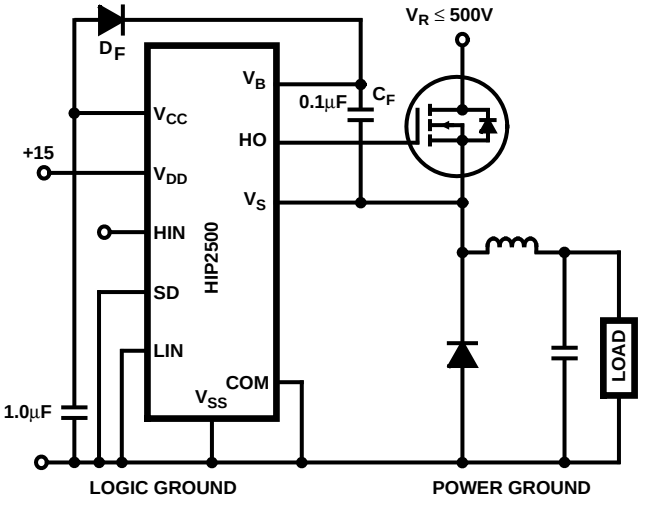


FIGURE 2. HIGH SIDE SWITCH OR “BUCK CONVERTERS”

Description of the HIP2500

The block diagram of the HIP2500 is shown in Figure 3. The HIP2500 contains both ground referenced and high voltage bus referenced (floating) gate drive circuits. With the exception of level-translation circuitry communicating between the upper driver circuit and the upper input control logic, the upper and lower driver and control circuits are nearly identical.

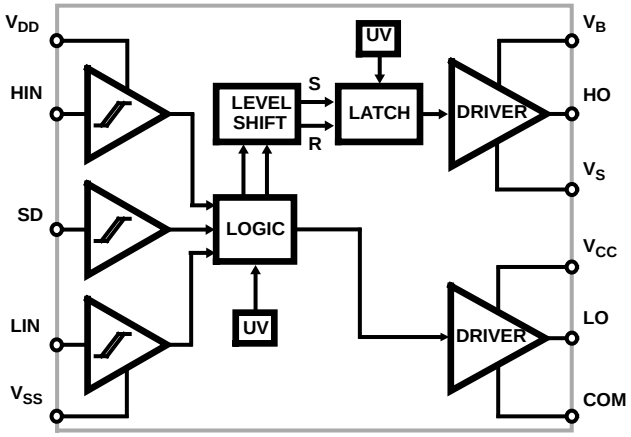


FIGURE 3. HIP2500 FUNCTIONAL BLOCK DIAGRAM

Input Logic

The input logic of the HIP2500 incorporates pull-down circuits which allow any of these inputs to be left open if they are not used. The pull-down current is approximately 12 micro-amps. As well as electrostatic input protection, the inputs are Schmitt-buffered and a level-translation circuit allows 5 volt logic inputs to communicate with the downstream logic which drives the gates of the power switches connected to the HIP2500. This logic is nominally biased between 12 and 15 volts. An extra benefit of the level-shifter is to provide input circuit noise immunity by continuing to function even though the V_{SS} terminal moves with respect to the COM terminal from about -2.0 volts to +VCC/2 volts. When attempting to lower the V_{SS} terminal more than -2.0 volts below COM, however, the HIP2500 will continue to function, but heavy substrate current flows. Therefore one should not attempt to deliberately shift the V_{SS} and COM terminals from each other.

The three inputs to the HIP2500; HIN, LIN and SD control the floating high side driver, the low side (ground referenced) driver and the “shutdown” functions, respectively, in accordance with the timing diagram in Figure 5. The HO and LO gate drive signals respond within a short (typically 400ns) propagation delay of their respective HIN and LIN signals. In half-bridges where deadtime is required to prevent conduction overlap or “shoot-through”, the HIN and LIN input commands must be appropriately spaced by the user. For example in a typical half-bridge configuration such as in Figure 4, where the upper and lower switches are series connected between the high and low sides of the power bus, the user must ensure that one switch is completely off before turning on the other. If this precaution is not followed, conduction overlap will occur in both switches, usually leading to destruction of one or both power switches and possibly the HVIC. Occasionally, a few passive components added to delay switch turn-on without delaying turn-off can effectively control shoot-through (see the diode resistor parallel combination in Figure 4). As power levels and power switch devices become larger, active rather than passive techniques may be a more appropriate means for providing turn-on blanking of one switch while turning off the other.

Two independent latches provide a means to inhibit the HO and LO outputs from going high whenever a Shutdown pulse has occurred. Resetting of the latches is accomplished at the moment that the respective HIN and LIN signals go low, provided that the SD input is also low.

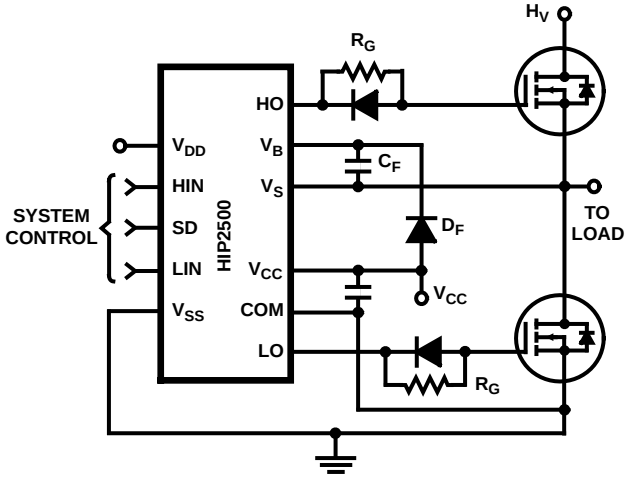


FIGURE 4. SIMPLIFIED SHOOT-THROUGH CONTROL

The timing diagram shown below will help to make operation of the input latch and shutdown logic more clear. The arrows

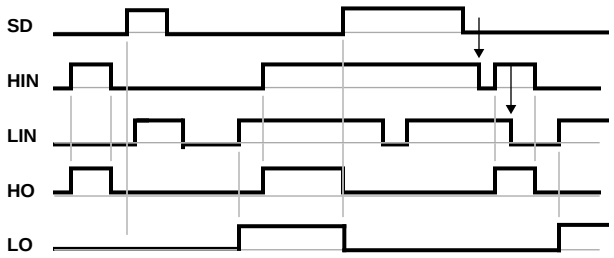


FIGURE 5. INPUT TIMING DIAGRAMS

show that at the instant the HIN and/or LIN inputs go low the shutdown latch is reset. Subsequent high signals on HIN or LIN will then be passed on to the edge logic and level-translation circuits before final processing by the output driver circuits.

Edge Logic

After the HIN and LIN input signals are squared up by the input logic, they are processed further by the Edge Logic. The purpose of the Edge Logic is to create short pulses to be further processed by the upper and lower output driver logic. There are two Edge circuits; one for the floating driver and one for the COM referenced driver.

Each Edge circuit has two inputs and two outputs. One output goes high coincident with a rising-edge signal from the input logic. The other output goes high coincident with a falling-edge signal from the input logic. Both outputs are short pulses which minimize the power dissipation of the Level-translation transistor. Although there is no lower level-translation transistor, the lower Edge circuit nonetheless helps provide the necessary symmetry between upper and lower switch delays. The second input to each Edge circuit comes from the lower Undervoltage (U/V) circuit. In the event of a lower undervoltage condition (i.e.: a low V_{CC}), the outputs of both upper and lower Edge circuits issue turnoff pulses.

Level-Translation

The upper Edge circuit issues turnon and turnoff pulses to the Level-Translation circuit. This circuit mainly consists of two high voltage npn transistors which conduct very narrow current pulses to the upper (floating) gate drive circuit.

Communication with the upper switch drive logic creates a potential for excessive power dissipation. By using only very short level-shift pulses from the V_{SS} referenced logic through the high voltage level-shift circuit to a latch in the upper switch driver, level-shifting power dissipation can be minimized. Two high voltage level-shift transistors are required to control the upper switch, one for turnon pulses and one for turnoff pulses. The level-shift current pulses are robust in order to provide noise discrimination, but are also very short so as to avoid significant power dissipation.

Driver Circuits

The driver circuits for the upper and lower gate drives are identical, except for the settings of the delay-matching circuits. Delay matching makes it easier to equalize the dead-time between upper and lower switch conduction periods. A secondary benefit of delay matching is to provide duty-cycle equalization of the input waveform and the output waveform at the V_S terminal. Delay-matching imbalance becomes more noticeable at high switching frequencies.

The HIP2500 uses p-channel mosfets in the output stage of the drivers for sourcing gate current to the power devices and is unique in its ability to drive the gates of the upper and lower switches to the full applied bias voltage. Similarly N-channel devices have been employed for sinking current from the gates of the power devices. This allows complete utilization of the supply voltage and power device gate voltage will be unaffected by changes in driver threshold voltage variations. The approach employed in the HIP2500 also avoids the additional power dissipated due to the threshold voltage drop associated with source-follower topologies. At high operating frequencies this can be significant.

The sink and source currents of the gate drivers are fully capable of supplying peak currents of at least 2.0A, which means that a power mosfet device with 3000pF gate source capacitance can be fully charged in 25ns. Discharge of the gate source capacitance will be slightly more rapid, since R_{DSon} of the sink driver is about 10% less than the source driver.

The high side driver section is built into an “isolation tub” which is capable of floating $+500V_{DC}$ above substrate potential with respect to power ground (COM pin 2). Pin 6 (V_S) is the common potential for the upper drive circuitry and is the most negative voltage within the floating tub. V_B (pin 5) is the positive rail within the floating tub and is usually 12 to 15 volts above V_S. The gate drive output, HO (pin 7) swings between V_S and V_B according to the state of the HIN input pin.

Under-Voltage Lockout

The HIP2500 is protected internally from insufficient bootstrap supply voltage (in the case of the upper floating driver) and insufficient bias supply voltage (in the case of the lower driver). Also the HIP2500 will not turn on either of the switches should the high voltage supply be brought up before the low voltage bias supply power.

As mentioned previously under Edge Logic, the lower undervoltage lockout blocks drive to both upper and lower power switches. The reason for turning off both switches when only the lower bias supply is below its U/V trip setpoint is that the upper bias supply is refreshed from the lower supply. Therefore the floating supply can never be any higher than the voltage on V_{CC}. The U/V latches are reset upon reestablishment of proper bias supply voltage level and a low transition of the LIN and/or HIN signals.

The upper logic circuit has a separate undervoltage circuit which controls only the gating of the upper (floating) switch. The switch is latched off upon occurrence of an undervoltage condition across the bootstrap capacitor. Latching is reset when the undervoltage condition goes away. A subsequent “on” pulse from the HIN terminal will turn on the upper switch. The HIN terminal must have previously gone low in order for the Edge circuit to issue an on pulse to the upper driver logic. Latching the drivers off in the event of an undervoltage condition eliminates the potential of entering a limit-cycle condition. To avoid U/V trip, the circuit designer must pick a value for bootstrap capacitance which supports the bias current requirements of the floating supply without tripping the under-voltage circuit. Guidance on choosing the bootstrap capacitor can be found under “Design Considerations” later in this note.

Design Considerations

The designer must deal with the following areas to successfully apply the HIP2500:

- Bias Supply Design
- Propagation Delay Issues
- Power Dissipation, Thermal Design

Bias Supply Design

The design of the HVIC bias supply is not particularly difficult. First establish the desired gate voltage for the power switch. For most MOSFETs and IGBTs there is a point at which increasing gate-to-source voltage yields no significant reduction in switch forward drop. Usually this occurs at about 8 to 9 volts. Avoid overcharging the gate of the power switch because the higher the gate voltage is the longer it takes to turn off the device. Also more charge must be transferred, which dissipates more power both in the HIP2500 and in the switch device. Finally, by increasing the time required to turn off the power MOS device, one increases the risk of "shoot-through". For all of the above reasons it is wise not to overcharge the gate of the power device.

Under-Voltage Requirements

The designer must pay attention to how low the Bias Supply voltage can go before causing the forward voltage drop of the power switch to increase dangerously. Generally, this voltage will be about 8 volts or less. The HIP2500 provides undervoltage protection at typically 9 volts, although the minimum trip value can be as low as 7.7 volts.

To reset the undervoltage circuit requires that the supply voltage exceed the trip level by at least 0.25 volts (the hysteresis of the U/V circuit). To again turn on a switch, a new edge signal must be generated by issuing a new high input on the desired input (HIN / LIN).

Lower Bias Supply Design

The lower bias supply design is simple, but must be clean and have low series resistance and inductance between the source and the VCC terminals. Also the common from the supply source to the COM terminal on the IC should be short and of low impedance. Usually it is sufficient to put a low ESR capacitor of a few microfarads directly from V_{CC} to COM. In any event, this capacitor must have sufficient charge to dump into the bootstrap capacitor whenever the VS (phase) terminal moves toward COM. This happens when the lower switch is on and usually whenever the upper switch has just been turned off. This will be explained in more detail under Bootstrap Circuit Design.

Another point to remember is that the voltage remaining on the bypass capacitor after dumping to the bootstrap capacitor should not cause the voltage on the bypass capacitor to drop below the Maximum undervoltage trip level. This level can be as high as 9.99 volts. Of course this assumes no current will come from the external bias supply during the refresh time. In practice, your supply will probably not be this soft and a good rule of thumb is to choose a bypass capacitor about 10 times larger than the bootstrap capacitance.

Bootstrap Circuit Design

The upper bias is maintained by the Bootstrap Capacitor between refresh cycles. A refresh cycle is defined as the time which elapses between conduction periods of the lower power switch and/or its body diode or flyback diode. Sometimes compromises on the size of the bootstrap capacitor must be made. For example, the capacitor should not be so large as to require an excessively long refresh period. Nor should it be so small that the voltage droops below the undervoltage trip point during the upper switch conduction period.

The largest factor in the amount of droop for frequencies above several KHz is the magnitude of charge required to charge the gate input capacitance of the driven switch to its final voltage. The charge lost by the bootstrap capacitor will be slightly larger than the charge acquired by the gate capacitance of the power switch as shown in (EQ. 1):

$$Q_G \approx (V_{BS1} - V_{BS2}) C_{BS} \quad \text{(EQ. 1)}$$

where:

V_{BS1} = C_{BS} voltage immediately after refresh
V_{BS2} = C_{BS} voltage immediately before refresh
C_{BS} = Bootstrap capacitance
Q_G = Turn-on Gate charge transferred

Figure 6 will help to understand the operation of the bootstrap circuit. The figure shows the refresh current paths which will charge the bootstrap capacitor to prepare it for driving the upper power switch. As previously stated, whenever the lower switch, its body diode or an external flyback diode conducts, the phase node (V_S) to which the load is connected, goes low toward the COM potential. The voltage at V_{CC} forces current through the bootstrap diode, the bootstrap capacitor and the lower switch/diode combination as shown by the arrows in Figure 6.

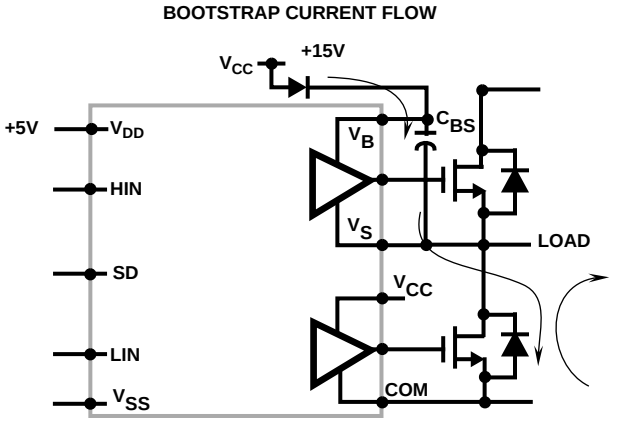


FIGURE 6. HVIC BOOTSTRAP CHARGING PATH

To charge the bootstrap capacitor quickly, without ringing or excessive overshoot, maintain a short, tight bootstrap refresh loop. This usually requires a low ESR decoupling capacitor located adjacent to HIP2500 from V_{CC} to COM and close positioning of the power switches to the HIP2500. The bootstrap capacitor and diode should also be located adjacent to the HIP2500 to aid in keeping this loop as short as possible, thereby minimizing the impedance of this loop.

To insure that the bootstrap capacitor voltage is maintained, it is usually necessary to turn on the lower switch each and every cycle of the PWM waveform. The duration of the refresh period should be long enough to guarantee that refreshing will be complete.

Relying on the lower freewheeling or body diode to provide refreshing without physically turning on the lower switch may fail to properly refresh the bootstrap capacitor under certain circumstances. This can happen when the load current is either zero or in a direction as to flow into the upper freewheel diode or body diode into the high voltage bus. Unless the lower power switch is turned on each cycle for the short refresh period, the bootstrap capacitor may not get refreshed. The conditions which can lead to this situation often occur in motor controls where the motor is coasting in one direction or the other at extremely light loads. Also controllers with a tendency to “over-modulate” can cause a refresh failure.

Users, anxious to get their circuit up and running quickly, will find that a ceramic bootstrap capacitor of approximately 0.1µF to 0.15µF will be sufficient to drive most small to medium size MOSFETs. The leadless surface-mount capacitors minimize series inductance and enhance rapid refreshing of this capacitor.

The bootstrap diode should be a small signal high voltage type capable of blocking full DC bus voltage plus the Vcc voltage. The recovery charge of the diode should be small so that when it recovers it will not appreciably discharge the bootstrap capacitor. Leakage current is usually not a concern, since the recovered charge of the diode will be much more significant than the leakage current over the PWM cycle. A 1000 volt signal diode, such as industry standard 1N5622, is preferable to a lower voltage diode, since its junction capacitance and recovered charge will be smaller. Also a higher voltage diode will have a low reverse leakage current when operated at half of its rated blocking voltage. Standard small signal diodes such as the 1N4000 series should be avoided. No rule of thumb will work in all situations, so it is usually better to take a more detailed look at all the factors which affect the bootstrap capacitor size.

The required value of capacitance depends on the Vcc voltage, the switching frequency, the HIP2500 high side supply current requirement, and the amount of equivalent gate capacitance or gate charge required to fully charge the gate. The gate charge requirement is generally included on most MOSFET data sheets. Figure 7 shows a curve for a Harris IRF450 MOSFET. By designing the bootstrap circuit to supply the total required gate charge shown on the MOSFET data sheet, the designer has included the effects of the Miller capacitance.

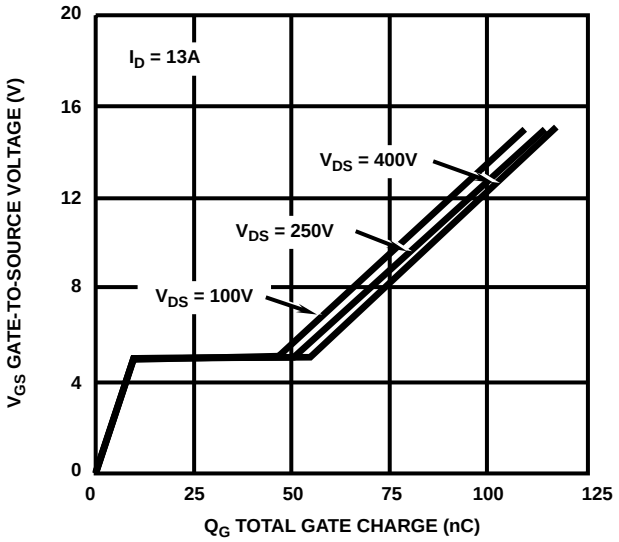


FIGURE 7. GATE CHARGE vs VOLTAGE

As previously mentioned, the layout of the bootstrap circuit should be compact so as to minimize the series inductance of the bootstrap circuit. Excessive inductance will interfere with rapidly charging the bootstrap capacitor during the time provided by the minimum off-time of the upper switch. The time allotted for turning off the upper switch is under full control of the circuit designer. However, maximum switching frequency and duty cycle requirements often forces the designer to live with “off-times” of less than 1 microsecond. As the allotted refresh time is forced lower and lower, the need for a short refresh loop becomes crucial.

A Real Example

A more exact sizing of the bootstrap capacitor than indicated by (EQ. 1) takes into account the upper bias supply current to the HIP2500 and leakage and recovery effects of the bootstrap diode. Obviously PWM frequency will affect the size requirement of the bootstrap capacitor too, so it would be valuable to include PWM frequency as well. If we define the following terms:

I_{DR} = Bootstrap diode reverse leakage current
I_{QBS} = Upper supply quiescent current
Q_{rr} = Bootstrap diode reverse recovered charge
Q_G = Turn-on Gate charge transferred
f_{PWM} = PWM operating frequency
V_{BS1} = C_{BS} voltage immediately after refresh
V_{BS2} = C_{BS} voltage immediately before refresh
C_{BS} = Bootstrap capacitance

then it will be possible to calculate a value for the bootstrap capacitor as shown in(EQ. 2):

$$C_{BS} = \frac{Q_G + Q_{rr} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \qquad \text{(EQ. 2)}$$

As an example, suppose we wish to drive an IRF450 to 15 volts allowing a droop of 0.5 volts over the PWM cycle (i.e.: V_{BS1}-V_{BS2}) with a 16 nano-coulomb recovery charge and a leakage current of 2 micro-amps for the bootstrap diode with a

maximum bias current, I_{QBS}, of 400 micro-amps. The gate charge, Q_G, of 120 nano-coulombs required to drive the IRF450 was read from the data sheet (see Figure 7). The desired PWM switching frequency will be 20KHz. Using (EQ. 2), one would need a bootstrap capacitance of at least 0.31 microfarads. Since 0.33 microfarads is the next larger standard capacitance available, a ceramic capacitor of this value will be chosen.

The length of the refresh time required to charge the bootstrap capacitor still needs to be evaluated. The refresh loop is comprised of the bootstrap capacitor, the bootstrap diode, stray circuit board resistance (the designer has laid out his circuit to minimize this and stray inductance) and the R_{DSON} of the power switch. The R_{DSON} of the IRF450 is approximately 0.3 ohms at 10 amps. To the above must be added the r_D of the bootstrap diode, which is about 1.1 ohms max. at 1.0 amp. Assuming another 0.1 ohm series resistance for the capacitor and circuit board traces, then a total resistance of about 1.5 ohms is in the bootstrap loop. The charge time constant of the bootstrap capacitor is the product of the loop resistance of 1.5 ohms and the bootstrap capacitance of 0.33 microfarads. This yields 0.5 seconds charging time constant. If 2 time constants are reserved for charging, then the bootstrap capacitor will only charge to about 86% of the V_{CC} supply. In 3 time constants it will charge to 95% of the V_{CC} supply. Keep in mind that the U/V circuit maximum trip level is 9.99 volts. This fact will impact the choice of capacitor and the allotted refresh time. If we assume 3 time constants are sufficient, then to drive the IRF450 to 15 volts would require a V_{CC} voltage of 15/95%, or 15.8 volts.

Propagation Delay Issues

The HIP2500 is designed to enhance rejection of noise from external circuits. Several filters and signal integrators are used to accomplish the noise rejection resulting in input to output propagation delays on the order of 400 nanoseconds. Much of the propagation delay associated with the upper switch is a result of the level-shift circuit. To better match the upper and lower propagation delays, additional delays were inserted in the lower circuit. Filter and matching circuits were designed to provide tracking of upper and lower propagation delays over temperature and bias voltage changes. In practice very good tracking is achievable, with the “on-delays” increasing approximately 150 nanoseconds over temperature and the “off-delays” increasing about 100 nanoseconds over temperature. Because the absolute propagation delays of the upper and lower circuits were not exactly matched, it is necessary to call attention to them so that the circuit designer can compensate for them.

The variation in propagation delays manifests itself in varying dead-times. Dead-time is defined as the time between the fall of one of the gate voltage waveforms and the rise of the other gate voltage waveform. The midpoints in the gate voltage waveforms are used to time the measurement. A 1000 picofarad load is used to simulate the “typical” power device gate-source load. It is possible, when turning off the upper and turning on the lower switch, to experience a slightly negative dead-time of less than 50 nanoseconds. The minimum dead-time experienced going the other way (turning off the lower and turning on the upper switch) is 95 nanoseconds. The best way to guarantee that proper dead-time always exists is to insure that the signals driving the LIN and HIN inputs of the HIP2500 always include dead-time. This will prevent shoot-through conduction and possible power device destruction. Dead-time can be enhanced by using the technique shown in Figure 4. With proper choice of series gate resistance, it may be possible to completely mask the effects of dead-time mismatch.

Power Dissipation and Thermal Design

The power dissipated in the HIP2500 can be lumped into static and dynamic losses. The static losses are limited to bias current losses for the upper and lower sections of the IC. The lower bias current, I_{QCC}, is typically 1.5 mA at +25°C. The upper bias current, I_{QBS}, is typically 300µA. At 15 volts bias, the total power dissipation is less than 30 milli-watts. Since I_{QDD} is typically only 100 pico-amps, the losses associated with this bias current is insignificant.

The switching losses are those losses associated with turning on and off the upper and lower power devices. These are the significant losses within the HIP2500. The switching losses can be further broken down into the following components:

- Low Voltage Gate Drive Charge Transfer
- High Voltage Level-Shifter
- High Voltage Tub-Capacitance Charge Transfer

The low voltage gate drive charge transfer power loss is the most significant of the 3 loss components above. (EQ. 3) describes the power loss attributable to the upper and lower switch gate charge transfer as a function of bias supply, V_{CC}, switching frequency, f_{PWM}, gate charge, Q_G, and the HIP2500 internal CMOS charge transfer losses, $Q_{internal}$, of the driver stages. Unless the gate charge of the power device is very small, $Q_{internal}$ is not very significant.

$$P_{SWLO} = 2f_{PWM}\left(Q_G + Q_{INTERNAL}\right)V_{CC} \quad \text{(EQ. 3)}$$

The high voltage level-shifter power dissipation, EQ. 4, is much more difficult to analyze. The reason that this equation is hard to solve is that the level-shift current pulses, i_{on} and i_{off}, and the phase voltage, v_{shift}, are all functions of time and the phase voltage moves in response to power switch turnon and turnoff, which is also dependent on the power MOSFET or IGBT used. The i_{on} pulse, for example, may come and go before any movement in the phase voltage is evident and therefore dissipate very little energy. The phase voltage usually will be a maximum when the i_{off} pulse comes, so the off pulse may dissipate quite a bit of energy.

$$P_{SHIFT} = \frac{1}{T}\int_0^T \left(i_{ON} + i_{OFF}\right)v_{SHIFT}\,dt \quad \text{(EQ. 4)}$$

Finally, the tub capacitance power dissipation can be calculated from EQ. 5. The “tub” is the p-n junction which isolates all of the circuitry associated with the high side driver from all

of the low side circuits. The calculation is a charge transfer energy calculation very similar to that used for the gate charge transfer, except that the charge is much smaller and the voltage, v_{shift}, much larger. This capacitance unfortunately varies with voltage and it is difficult to measure. The tub capacitance charge transfer losses are shared between resistances both internal and external to the HIP2500. A conservative approach, however, assumes all of the losses are dissipated within the HIP2500.

$$P_{TUB} = C_{TUB} V^2_{SHIFT} f_{PWM} \quad \text{(EQ. 5)}$$

Power Dissipation The Easy Way

Fortunately there is a much easier method available for measuring power dissipation and none of the above equations ever need to be evaluated. Very simple lab equipment can be used to obtain the measurements and simple calculations can be used to obtain accurate results.

The simple method for evaluating power dissipation breaks down the total power dissipation problem into high voltage power dissipation and low voltage power dissipation.

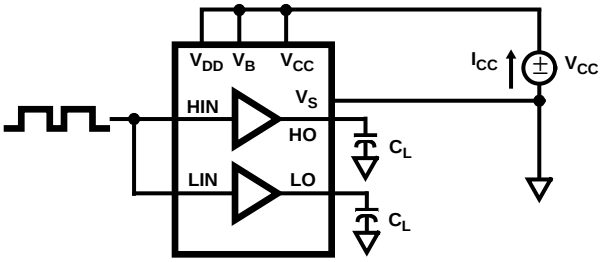


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

Low Voltage Power Dissipation

The low voltage power dissipation includes low voltage leakage and switching losses associated with gating both of the power switches. It also includes the CMOS switching losses associated with both driver stages. As shown in Figure 8, the upper and lower bias supplies are tied together and supplied by bias voltage V_{CC}, while capacitors C_L are tied to both of the HIP2500 outputs. Both inputs are then pulsed at the frequency of interest and the average current, I_{CC} is measured. The total low voltage power dissipation is then simply the product of I_{CC} and V_{CC} as shown in EQ. 6 below:

$$P_{LV} = V_{CC} I_{CC} \quad \text{(EQ. 6)}$$

Plotting the results of EQ. 6 as a function of switching frequency and the load capacitance of each of the power switches yields a family of curves for the low voltage power dissipation of the HIP2500 as shown in Figure 9.

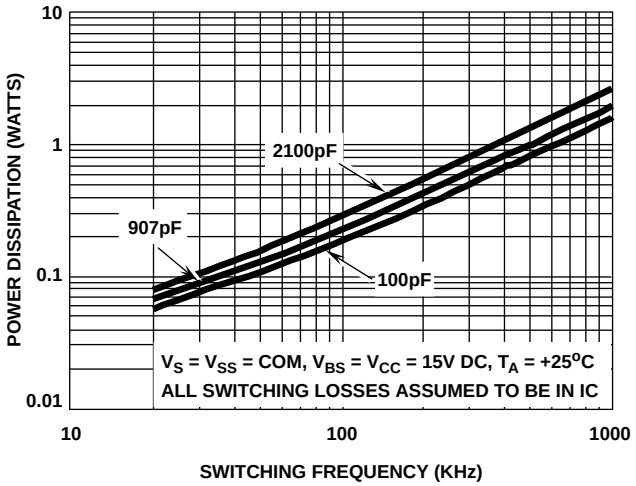


FIGURE 9. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

If the quiescent bias current and CMOS switching losses are subtracted from the above power calculation, what is left is the power required to drive the gate-source capacitance of the power switches. The power required from V_{CC} to drive the gates can also be calculated by EQ. 7, where C_G is the combined equivalent gate capacitance of both power switches. Half of this power is dissipated in the combined source resistance of the driver and any external resistance in the source circuit and the other half of the power is dissipated in the sinking circuit, including any external resistance in the sinking path.

$$P_G = V^2_{CC} C_G f_{PWM} \quad \text{(EQ. 7)}$$

High Voltage Power Dissipation

The high voltage power dissipation component includes the losses associated with the level-shifter and the tub charge transfer power losses. This component is not affected by the size of the power device being switched. Figure 9 shows the test circuit which is used to measure the high voltage level-shifter and high voltage leakage power losses.

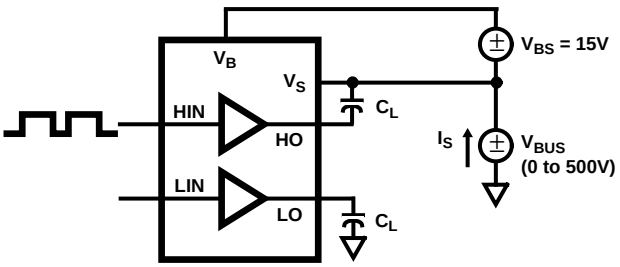


FIGURE 10. HIGH VOLTAGE POWER DISSIPATION TEST CIRCUIT

By measuring I_S and V_{BUS} and calculating the product of these measurements, one can obtain the value for total high voltage power loss for the HIP2500. The value derived will include both reverse leakage power due to the isolation tub and two level-shift events. Both the turnon level-shift and the turnoff level-shift events are included. The high voltage power dissipation will increase directly with both switching frequency and bus voltage level as shown in Figure 11.

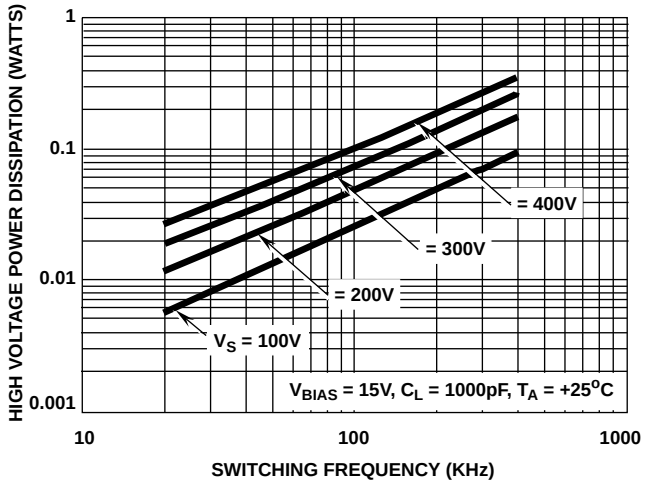


FIGURE 11. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY

Layout Issues

While a lot of effort was spent in designing the HIP2500 to be immune to noise, poor layout can cause problems.

Particular attention should be paid to keeping the distance between the HIP2500 and the power switches as short as possible. If your design is experiencing any of these effects, it may be helpful to first look at the possible causes in the table: Layout Problems and Effects.

Layout Problems and Effects

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance can cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead (V_S) causing V_S to ring excessively below the COM terminal causing possible malfunction of the HIP2500 due to excessive charge being pulled out of the substrate.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing Miller Effect when an opposing switch is being rapidly turned on.
Floating VSS with respect to COM. These should be tied together.	Can cause drive pulses to disappear or excessive current flow between V_{SS} and COM.

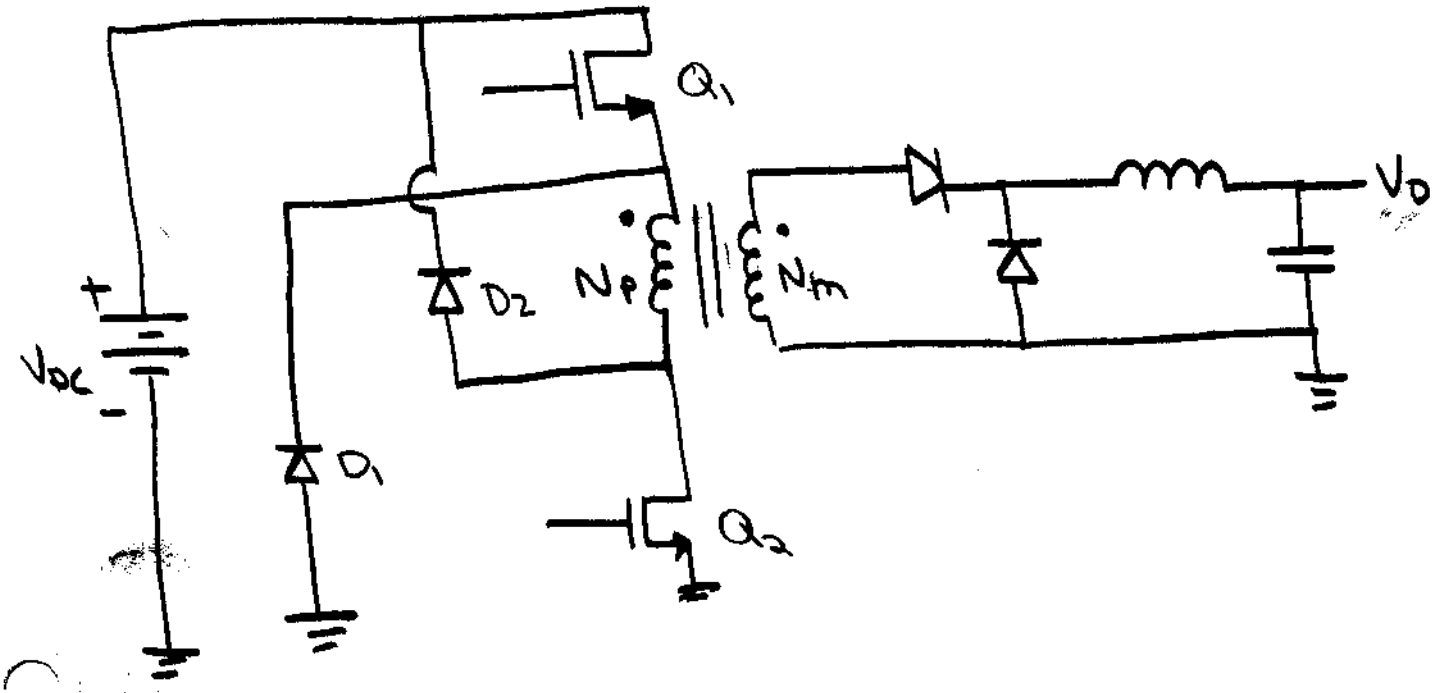
Quick Help Table

To aid in locating possible solutions to problems which can occur in applying the HIP2500 and similar high voltage IC gate-drivers, the following table is included.

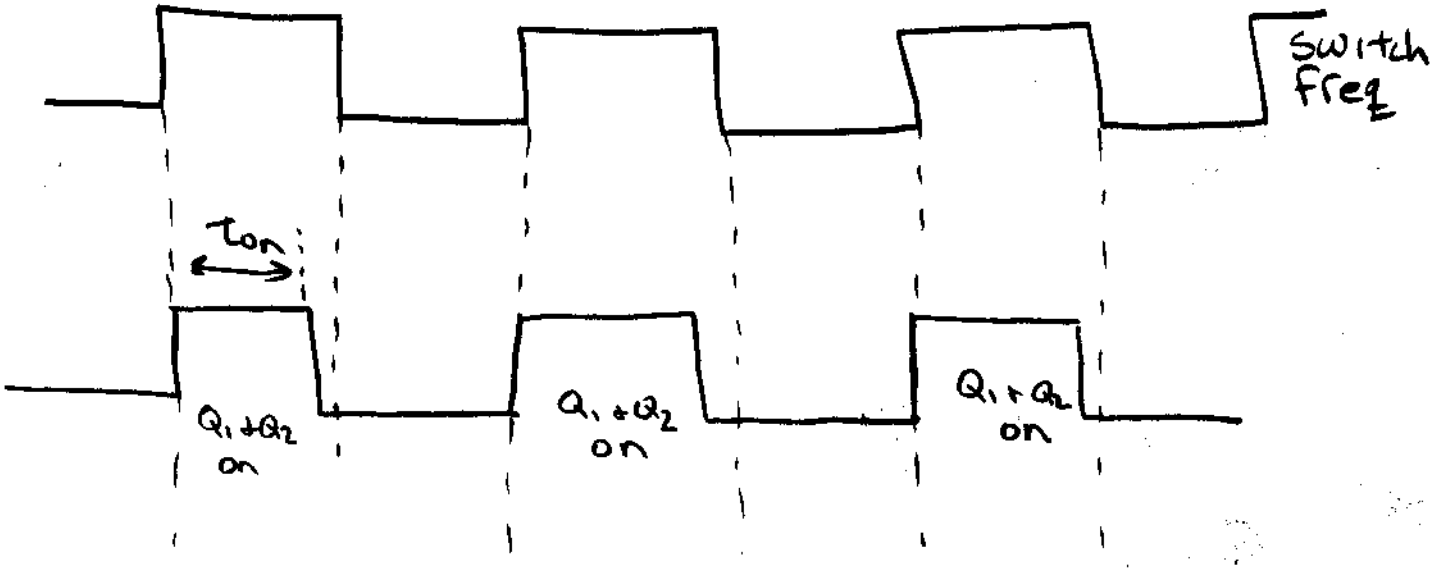
General Problems and Effects

PROBLEM	EFFECT
Low V_{DD} and V_{BS}	Low supply voltages can cause U/V lockout and blocking of gate drive.
High V_{DD} and V_{BS}	Causes wasted bias supply power due to overcharging the gates of the external switches and can result in reduced reliability due to decreased voltage margin to Max. bias voltage rating and increased operating temperature of the IC.
C_F too small	Insufficient charge to drive external power devices and/or possible U/V lockout can occur.
C_F too large	The bootstrap capacitor may not charge sufficiently to overcome U/V lockout level and gate drive never occurs. Either decrease C_F or increase the refresh time allotted to charge C_F.
R_{GATE} too big	R_{GATE} x C_F time constant too long causing excessive power device switching losses. Also R_{GATE} too big may fail to hold gate low when the opposing power device turns on, tending to either turn on the device prematurely or slow desired turn-off, due to the Miller Effect. May need to bypass R_{GATE} with an anti-parallel signal diode.
R_{GATE} too small	R_{GATE} too small tends to reduce effective dead time and increase shoot-through tendency. Also switching dv/dt increases EMI.
Negative or insufficient dead-time	Can cause external power devices and the IC to fail, possibly destroying circuit board traces also. This also tends to severely reduce “refresh” time (see C_F too large, above).
HIP2500 IC gets too hot	Trying to drive too large an external power device. Reduce the switching frequency, the high voltage bus or find a power device with a lower equivalent gate capacitance. You may also be able to increase air flow over the IC and/or add heat-sinking.
Unexplained arcing in vicinity of pins 3, 4 and 5 of IC	Poorly cleaned, dirty or improper attention to strike and creepage distances for the bus voltage level being used may cause this damage or similar damage between traces going to these points.

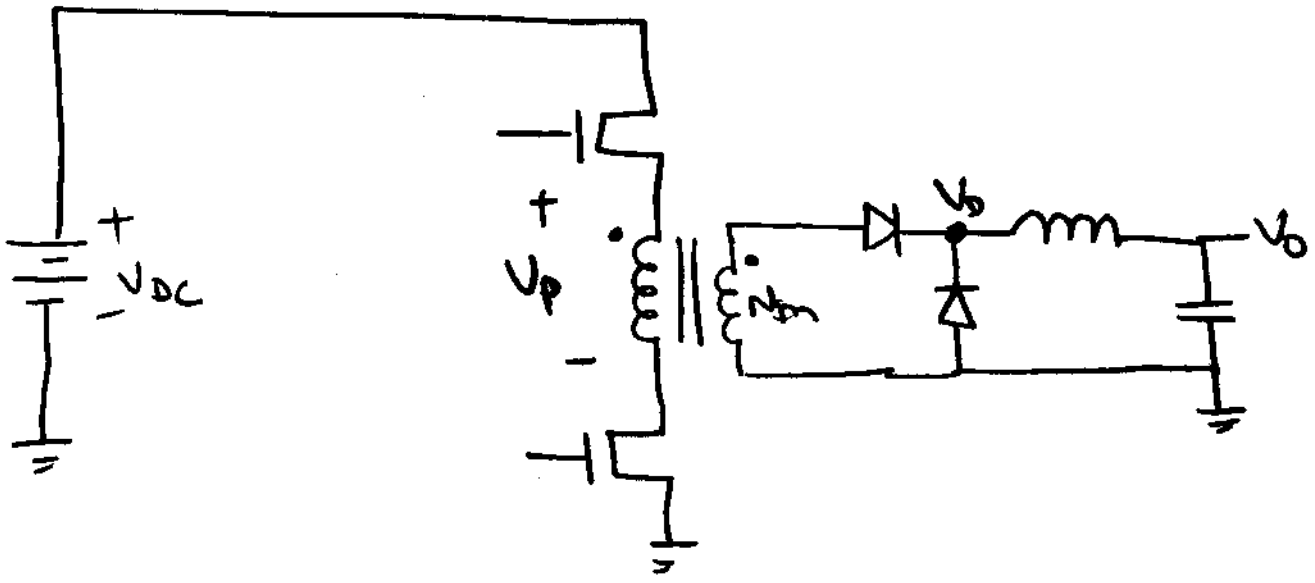
Double ended forward Converter



Q1 + Q2 are on and off at the same times



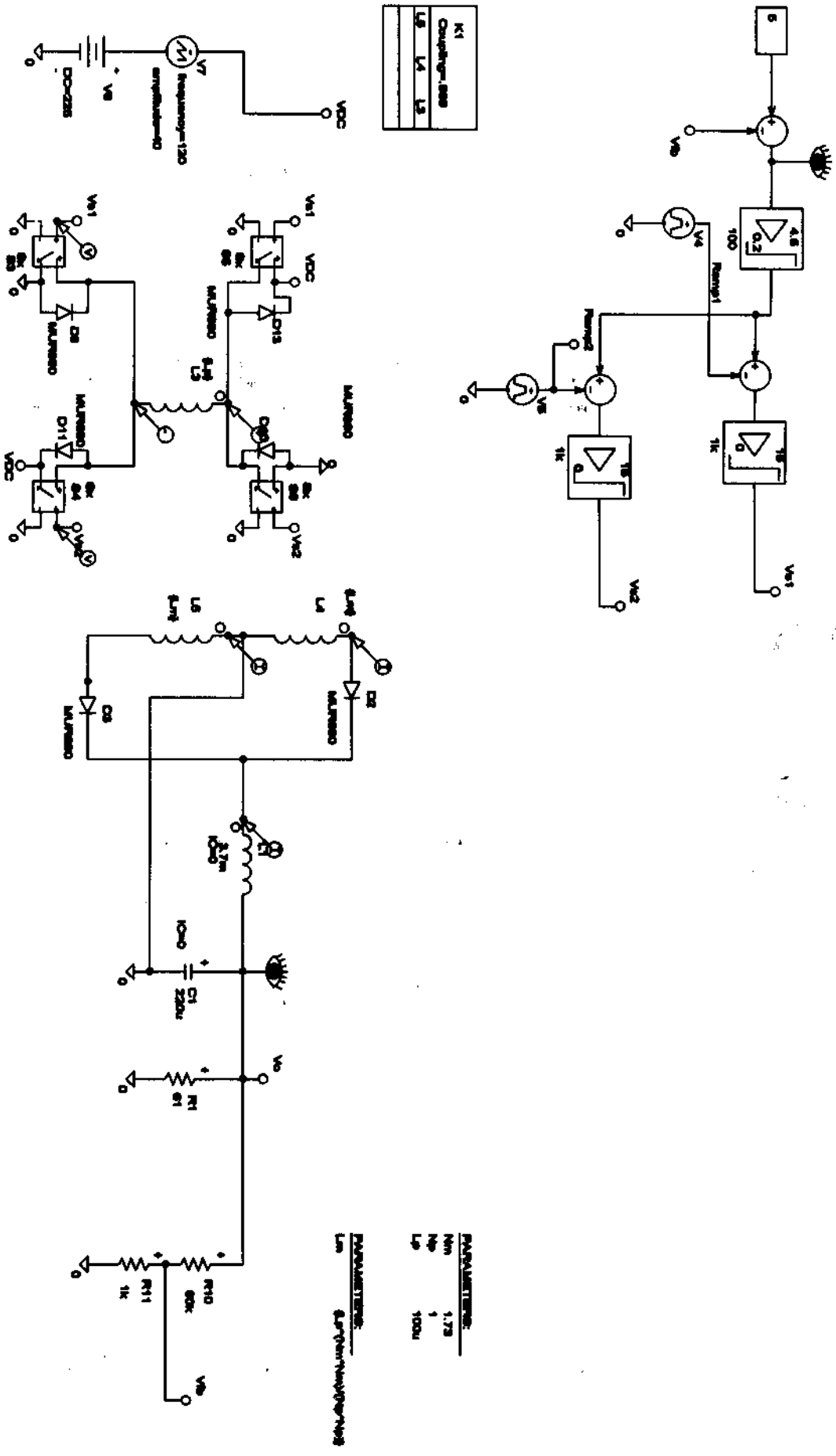
When Q_1 & Q_2 = on, Diodes are off



$$V_p = V_{DC} - 2V_{sw on}$$

$$V_D = \left[(V_{DC} - 2V_{sw on}) \frac{N_m}{N} - V_{D on} \right]$$

When switches turn off, current must continue to flow through the Primary



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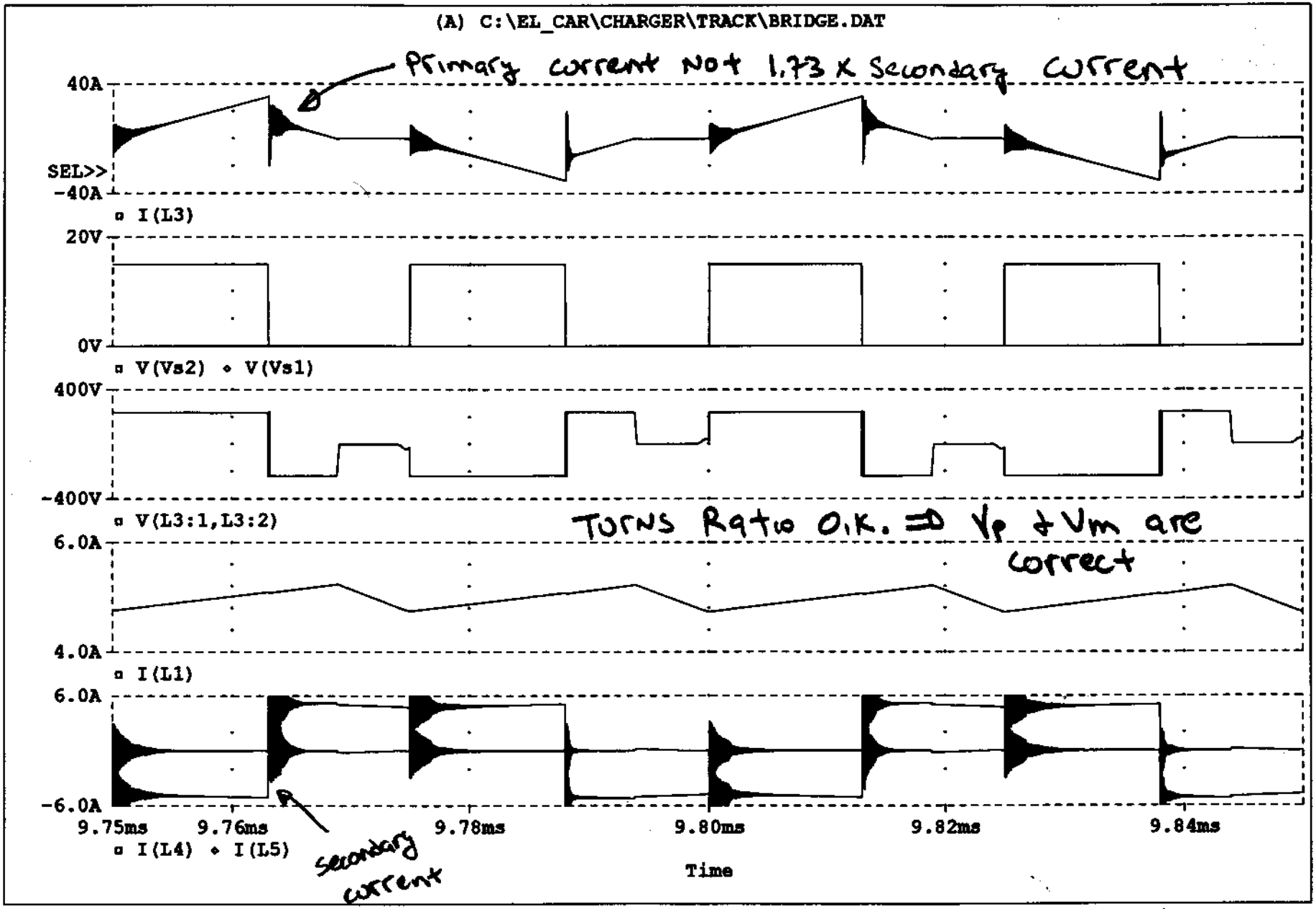

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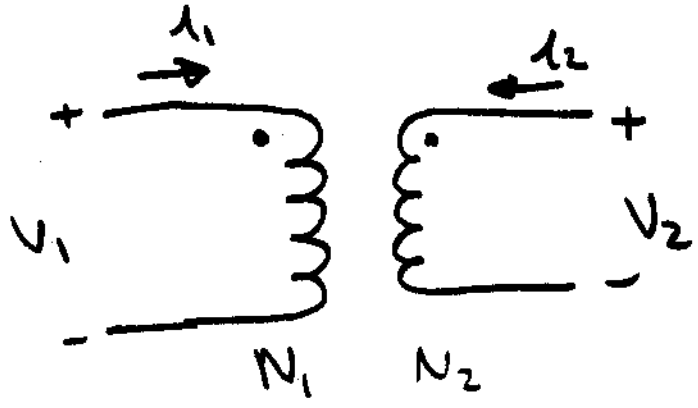
Making Transformers Ideal



Let $N = N_2/N_1$ $\qquad k = \frac{m}{\sqrt{L_1 L_2}}$

$$V_1 = L_1 \frac{di_1}{dt} + m \frac{di_2}{dt} \quad (1)$$

$$V_2 = m \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \quad (2)$$

First Find the relationship between V_1 and V_2

- Solve eq (2) for $\frac{di_2}{dt}$

$$\frac{di_2}{dt} = \frac{V_2}{L_2} - \frac{m}{L_2} \frac{di_1}{dt}$$

Plug into eq ①

$$V_1 = L_1 \frac{di_1}{dt} + \frac{m}{L_2} V_2 - \frac{m^2}{L_2} \frac{di_1}{dt}$$

$$V_1 = \left(L_1 - \frac{m^2}{L_2}\right) \frac{di_1}{dt} + \frac{m}{L_2} V_2$$

Now Remember $K = \frac{m}{\sqrt{L_1 L_2}} \Rightarrow m^2 = K^2 L_1 L_2$

$$m = K\sqrt{L_1 L_2}$$

Plug in

$$V_1 = \left(L_1 - \frac{K^2 L_1 L_2}{L_2}\right) \frac{di_1}{dt} + \frac{K\sqrt{L_1 L_2}}{L_2} V_2$$

OR

$$V_1 = \underbrace{L_1 (1-K^2) \frac{di_1}{dt}}_{\text{Don't Want}} + \underbrace{K\sqrt{\frac{L_1}{L_2}}}_{\text{Term we Want}} V_2 \quad ③$$

Leakage inductance

- To make V_1 & V_2 relationship Ideal

  Let $K \to 1$

- Does eq ③ say anything about how big L_1 & L_2 should be? L_1 = small

⇒ For Ideal Voltage Characteristics, $V_2 = \frac{N_2}{N_1} V_1$

We Need $K \to 1$. Size of L_1 & L_2 Do Not affect V_2 & V_1.

⇒ Question: for a 2:1 XFMR should we use

$N_2 = 2, N_1 = 1$,

$N_2 = 20, N_1 = 10$

$N_2 = 200, N_1 = 100$

$N_2 = 2000, N_1 = 1000$?

⇒ Not determined by equation

Look at eq ③ with $K=1$

$$V_1 = \sqrt{\frac{L_1}{L_2}}\, V_2$$

we like to use the equations

$$V_1 = \frac{N_1}{N_2} V_2$$

$$\Rightarrow N_1 = \sqrt{L_1}\,, \quad N_2 = \sqrt{L_2}\,, \quad \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}}$$

Normally we use

$$V_1 = \frac{N_1}{N_2} V_2 \qquad (4)$$

$$L_1 = \left(\frac{N_1}{N_2}\right)^2 L_2$$

- How much Ideality do we have?
- How big is $L_1(1-k^2)\frac{di_1}{dt}$ compared to $k\sqrt{\frac{L_1}{L_2}}\,V_b$?

- Look at a 2:1 XFMR, $N_2 = 2$, $N_1 = 1$
  use $k = 0.95$, $L_1 = 100\,mH$, $\Delta i/\Delta t = 1A/25\mu s$, $V_2 = 15V$

$$V_1 = L_1(1-k^2)\frac{di_1}{dt} + k\sqrt{\frac{L_1}{L_2}}\,V_2$$

$$= \underbrace{100mH\left(1-(0.95)^2\right)\frac{1A}{25\mu s}}_{390} + \underbrace{0.95\,\frac{1}{\sqrt{2}}\,15}_{7.125}$$

We need

$$L_1(1-k^2)\frac{di_1}{dt} << k\sqrt{\frac{L_1}{L_2}}\,V_2$$

OR

$$L_1 (1-k^2) \frac{di}{dt} << kV_1$$

$$L_1 << \left(\frac{k}{1-k^2}\right) \frac{V_1}{di/dt}$$

Now Find $i_1(t)$ from $i_2(t)$

Add eq ① + ②

$$V_1 + V_2 = (L_1 + m)\frac{di_1}{dt} + (m + L_2)\frac{di_2}{dt}$$

$$\frac{di_1}{dt} = \left(\frac{V_1 + V_2}{L_1 + m}\right) + \left(\frac{m + L_2}{m + L_1}\right)\frac{di_2}{dt}$$

Sub in $m = k\sqrt{L_1 L_2}$

$$\frac{di_1}{dt} = \frac{V_1 + V_2}{L_1 + k\sqrt{L_1 L_2}} + \left(\frac{L_2 + k\sqrt{L_1 L_2}}{L_1 + k\sqrt{L_1 L_2}}\right)\frac{di_2}{dt}$$

Look at $\dfrac{L_2 + k\sqrt{L_1 L_2}}{L_1 + k\sqrt{L_1 L_2}}$

$$\frac{L_2 + K\sqrt{L_1 L_2}}{L_1 + K\sqrt{L_1 L_2}} = \frac{L_2\left(1 + K\frac{\sqrt{L_1 L_2}}{L_2}\right)}{L_1\left(1 + K\frac{\sqrt{L_1 L_2}}{L_1}\right)}$$

$$= \frac{L_2}{L_1}\left(\frac{1 + k\sqrt{\frac{L_1}{L_2}}}{1 + k\sqrt{\frac{L_2}{L_1}}}\right)$$

Remember $\frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}}$

So we get

$$= \frac{N_2^2\left(1 + K\frac{N_1}{N_2}\right)}{N_1^2\left(1 + K\frac{N_2}{N_1}\right)}$$

$$= \frac{N_2(N_2 + kN_1)}{N_1(N_1 + KN_2)}$$

$$= \frac{N_2}{N_1} \text{ as } K \to 1$$

So we have

$$\frac{d\lambda_1}{dt} = \frac{V_1 + V_2}{L_1\left(1 + k\frac{N_2}{N_1}\right)} + \frac{N_2\left(N_2 + kN_1\right)}{N_1\left(N_1 + kN_2\right)} \frac{d\lambda_2}{dt}$$

Let $K \to 1$

$$\frac{d\lambda_1}{dt} = \frac{V_1 + V_2}{L_1\left(1 + \frac{N_2}{N_1}\right)} + \frac{N_2}{N_1} \frac{d\lambda_2}{dt}$$

Now use $V_2 = \frac{N_2}{N_1} V_1$

$$\frac{d\lambda_1}{dt} = \frac{\left(V_1 + V_1 \frac{N_2}{N_1}\right)}{L_1\left(1 + \frac{N_2}{N_1}\right)} + \frac{N_2}{N_1} \frac{d\lambda_2}{dt}$$

OR

$$\frac{d\lambda_1}{dt} = \frac{V_1}{L_1} + \frac{N_2}{N_1} \frac{d\lambda_2}{dt}$$

Integrate

$$\lambda_1(t) = \int_0^{t_{on}} \frac{V_1}{L_1}\,dt + \frac{N_2}{N_1}\lambda_2(t)$$

$$\lambda_1(t) = \underbrace{\frac{V_1}{L_1} t_{on}}_{\text{don't want}} + \underbrace{\frac{N_2}{N_1}\lambda_2(t)}_{\text{want}} \quad (5)$$

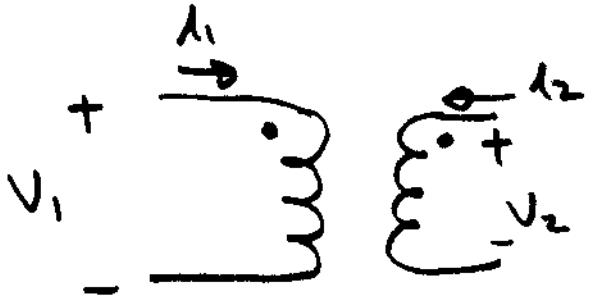
For Ideal XFMR, we need

$$\frac{V_1}{L_1} t_{on} \ll \underbrace{\frac{N_2}{N_1}\lambda_2(t)}_{\lambda_1(t) \text{ in ideal case}}$$

So we need

$$L_1 \gg \frac{V_1}{I_1} t_{on} \quad (6)$$

Transformer Summary



$$V_1 = L_1 \frac{d\lambda_1}{dt} + m \frac{d\lambda_2}{dt}$$

$$V_2 = m \frac{d\lambda_1}{dt} + L_2 \frac{d\lambda_2}{dt}$$

$$V_1 = \underbrace{L_1 (1-k^2) \frac{d\lambda_1}{dt}}_{\text{Leakage}} + k\sqrt{\frac{L_1}{L_2}}\, V_2$$

$$V_1 = \frac{N_1}{N_2} V_2 \,, \quad I_1 = \frac{N_2}{N_1} I_2, \quad \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}}$$

$$L_1 = \left(\frac{N_1}{N_2}\right)^2 L_2 \qquad \left(\frac{k}{1-k^2}\right)\frac{V_1}{d\lambda_1/dt} \gg L_1 \gg \frac{V_1}{I_1} t_{on}$$

$$\lambda_1(t) = \int_0^{t_{on}} \frac{v_1}{L_1}\, dt + \frac{N_2}{N_1} \lambda_2(t)$$