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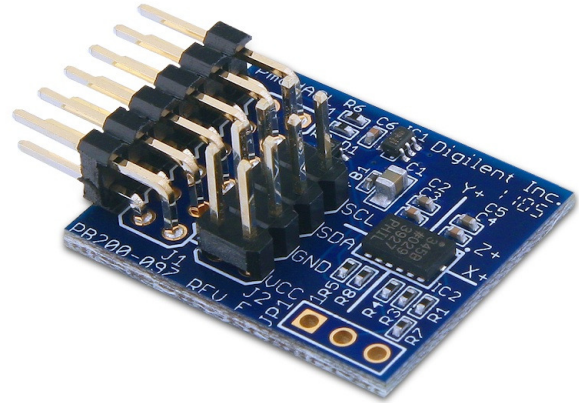
Note: This document applies to REV E of the board.

## Overview

The PmodACL is a 3-axis digital accelerometer module powered by the Analog Devices ADXL345.

Features include:

- user-selectable resolution
- single-tap/double-tap detection
- activity/inactivity monitoring
- free fall detection
- SPI and I<sup>2</sup>C interfaces



## Functional Description

The PmodACL uses a standard 12-pin connector and can communicate via SPI or I<sup>2</sup>C. A pull-up resistor on the ~SS line keeps the ADXL345 in I<sup>2</sup>C mode unless the host drives the line low, in which case the device will communicate via SPI.

## Interface

All communications with the device must specify a register address and a flag indicating whether the communication is a read or a write. This is followed by the actual data transfer.

Device configuration is performed by writing to control registers within the device.

Accelerometer data is accessed by reading device registers.

A full list of registers and their functionality, as well as communication specifications, is found in the ADXL345 datasheet available on the Analog Devices website.

### Interface Connector Signal Description

Connector J1 – SPI Communications		
Pin	Signal	Description
1	~SS	Slave Select
2	MOSI / SDA	SPI Master out Slave in Data / I <sup>2</sup> C Data
3	MISO	SPI Master in/Slave out Data
4	SCLK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V)
7	INT2	Interrupt 2
8	INT1	Interrupt 1
9	NC	Not Connected
10	NC	Not Connected
11	GND	Power Supply Ground
12	VCC	Power Supply (3.3V)

The SPI interface standard uses four signal lines. These are slave select (~SS), master out slave in (MOSI), master in slave out (MISO), and serial clock (SCLK). These signals map to the following signals on the ADXL345: ~SS corresponds to the Chip Select signal (~CS), MOSI corresponds to Serial Data Input (SDI), MISO corresponds to Serial Data Output (SDO), and SCK corresponds to the Serial Clock signal (SCLK).

<b>Connector J2 – I<sup>2</sup>C Communications</b>		
<b>Pin</b>	<b>Signal</b>	<b>Description</b>
1, 2	SCLK	Serial Clock
3, 4	SDA / SDI / SDIO	I <sup>2</sup> C Data / SPI Master out Slave in Data
5, 6	GND	Power Supply Ground
7, 8	VCC	Power Supply (3.3V)

The I<sup>2</sup>C interface standard uses two signal lines. These are I<sup>2</sup>C data (SDA) and serial clock (SCLK). These signals map to the serial data (SDA) and serial clock (SCLK) respectively on the ADXL345.