library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

datatype clockDivider is
    Port ( CLK : in STD_LOGIC;
            refreshClock : out STD_LOGIC;
            clockDig1 : out STD_LOGIC);
end clockDivider;

architecture Behavioral of clockDivider is

    signal count1: integer:=0;
    signal count2: integer:=0;
    signal tmp1 : std_logic:='0';
    signal tmp2 : std_logic:='0';

begin

    frequencyDivider : process(CLK)
    begin
        if rising_edge(CLK) then
            count1 <= count1+1;
            count2 <= count2+1;
            if (count1 = 208334) then
                tmp1 <= NOT tmp1;
                count1 <= 0;
            end if;
            if (count2 = 500000) then
                tmp2 <= NOT tmp2;
                count2 <= 0;
            end if;
        end if;
    end process;

    refreshClock <= tmp1;
    clockDig1 <= tmp2;
end Behavioral;