ULN2803A Darlington Transistor Arrays

1 Features
- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications
- Compatible with ULN2800A Series

2 Applications
- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description
The ULN2803A device is a high-voltage, high-current Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A device has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

4 Simplified Schematics

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE (PIN)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803</td>
<td>SOIC (18)</td>
<td>11.50 mm × 7.50 mm</td>
</tr>
<tr>
<td></td>
<td>PDIP (18)</td>
<td>22.48 mm × 6.35 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
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5 Revision History

Changes from Revision F (January 2014) to Revision G Page

• Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1

Changes from Revision E (July 2006) to Revision F Page

• Updated document to new TI data sheet format - no specification changes. ................................................................. 1
• Deleted Ordering Information table. ............................................................................................................................... 1
## 6 Pin Configuration and Functions

![DW OR N PACKAGE (TOP VIEW)](image)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;1:8&gt;B</td>
<td>I</td>
<td>Channel 1 through 7 darlington base input</td>
</tr>
<tr>
<td>&lt;1:8&gt;C</td>
<td>O</td>
<td>Channel 1 through 7 darlington collector output</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>Common Emitter shared by all channels (typically tied to ground)</td>
</tr>
<tr>
<td>COM</td>
<td>I/O</td>
<td>Common cathode node for flyback diodes (required for inductive loads)</td>
</tr>
</tbody>
</table>
# Specifications

## 7.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter voltage</td>
<td>50</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage(^{(2)})</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Peak collector current</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Total substrate-terminal current</td>
<td>–2.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Operating virtual junction temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

## 7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_I)</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CC})</td>
<td>0</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>(T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

## 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>ULN2803A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA})</td>
<td>73</td>
<td>18 PINS</td>
</tr>
<tr>
<td>(R_{JC(top)})</td>
<td>40.3</td>
<td>18 PINS</td>
</tr>
<tr>
<td>(R_{JB})</td>
<td>38.9</td>
<td>18 PINS</td>
</tr>
<tr>
<td>(\psi_{JT})</td>
<td>10.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB})</td>
<td>38.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(bot)})</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the **IC Package Thermal Metrics** application report, SPRA953.
7.5 Electrical Characteristics

at $T_A = 25^\circ C$ free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>ULN2803A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CEX}$</td>
<td>$V_{CE} = 50 \text{ V}$, see Figure 4</td>
<td></td>
<td>50 $\mu\text{A}$</td>
</tr>
<tr>
<td>$I_{(\text{off})}$</td>
<td>$V_{CE} = 50 \text{ V}$, $T_A = 70^\circ C$, see Figure 5</td>
<td>50</td>
<td>65 $\mu\text{A}$</td>
</tr>
<tr>
<td>$I_{(\text{on})}$</td>
<td>$V_I = 3.85 \text{ V}$, see Figure 6</td>
<td>0.93</td>
<td>1.35 mA</td>
</tr>
<tr>
<td>$V_{(\text{on})}$</td>
<td>$V_{CE} = 2 \text{ V}$, see Figure 7</td>
<td>$I_C = 200 \text{ mA}$</td>
<td>2.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 250 \text{ mA}$</td>
<td>2.7 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 300 \text{ mA}$</td>
<td>3 V</td>
</tr>
<tr>
<td>$V_{CE(\text{sat})}$</td>
<td>$I_I = 250 \mu\text{A}$, see Figure 8</td>
<td>$I_C = 100 \text{ mA}$</td>
<td>0.9 1.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 350 \mu\text{A}$, see Figure 8</td>
<td>1 1.3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 500 \mu\text{A}$, see Figure 8</td>
<td>1.3 1.6 V</td>
</tr>
<tr>
<td>$I_R$</td>
<td>$V_R = 50 \text{ V}$, see Figure 9</td>
<td></td>
<td>50 $\mu\text{A}$</td>
</tr>
<tr>
<td>$V_F$</td>
<td>$I_F = 350 \text{ mA}$, see Figure 10</td>
<td></td>
<td>1.7 2 V</td>
</tr>
<tr>
<td>$C_i$</td>
<td>$V_I = 0$, $f = 1 \text{ MHz}$</td>
<td></td>
<td>15 25 $\text{pF}$</td>
</tr>
</tbody>
</table>

7.6 Switching Characteristics

$T_A = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>$V_S = 50 \text{ V}$, $C_L = 15 \text{ pF}$, $R_L = 163 \Omega$, see Figure 11</td>
<td>130</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$V_S = 50 \text{ V}$, $I_O = 300 \text{ mA}$, see Figure 12</td>
<td>20</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$V_S = 50 \text{ V}$, $I_O = 300 \text{ mA}$, See Figure 12</td>
<td>$V_S = 20$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

7.7 Typical Characteristics

![Typical Characteristics Graphs]
Typical Characteristics (continued)

Figure 3. Output Current vs Input Current

- $R_L = 10 \, \Omega$
- $T_A = 25 \, ^\circ C$
- $V_S = 10 \, V$
- $V_S = 8 \, V$

$I_C$ – Collector Current – mA

$I_I$ – Input Current – mA

Figure 3. Output Current vs Input Current
8 Parameter Measurement Information

Figure 4. $I_{CEX}$ Test Circuit

Figure 5. $I_{(off)}$ Test Circuit

Figure 6. $I_{(on)}$ Test Circuit

Figure 7. $V_{I(on)}$ Test Circuit

Figure 8. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

Figure 9. $I_R$ Test Circuit

Figure 10. $V_F$ Test Circuit
Parameter Measurement Information (continued)

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
B. $C_L$ includes probe and jig capacitance.
C. $V_{IH} = 3$ V

Figure 11. Propagation Delay-Times
Parameter Measurement Information (continued)

Test Circuit

Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_0 = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 12. Latch-Up Test
9  Detailed Description

9.1  Overview
This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 8 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803A comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803A has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The ULN2803A offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

9.2  Functional Block Diagram

9.3  Feature Description
Each channel of ULN2803A consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain ($\beta$). This can be as high as 10,000 A/A at certain currents. The very high $\beta$ allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 kΩ & 3.0 kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4  Device Functional Modes

9.4.1  Inductive Load Drive
When the COM pin is tied to the coil supply voltage, ULN2803A is able to drive inductive loads and suppress the kick-back voltage via the internal free wheeling diodes.

9.4.2  Resistive Load Drive
When driving a resistive load, a pull-up resistor is needed in order for ULN2803A to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
ULN2803A will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803A, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in Figure 13.

10.2 Typical Application

Figure 13. ULN2803A as Inductive Load Driver
Typical Application (continued)

10.2.1 Design Requirements
For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Voltage</td>
<td>3.3 V or 5.0 V</td>
</tr>
<tr>
<td>Coil Supply Voltage</td>
<td>12 V to 100 V</td>
</tr>
<tr>
<td>Number of Channels</td>
<td>8</td>
</tr>
<tr>
<td>Output Current (R\textsubscript{COIL})</td>
<td>20 mA to 300 mA per channel</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>100%</td>
</tr>
</tbody>
</table>

10.2.2 Detailed Design Procedure
When using ULN2803A in a coil driving application, determine the following:
• Input Voltage Range
• Temperature Range
• Output & Drive Current
• Power Dissipation

10.2.2.1 Drive Current
The coil current is determined by the coil voltage (VSUP), coil resistance & output low voltage (V\textsubscript{OL} or V\textsubscript{CE(SAT)}).

\[
I_{\text{COIL}} = \frac{(V_{\text{SUP}} - V_{\text{CE(SAT)}})}{R_{\text{COIL}}}
\]  

(1)

10.2.2.2 Output Low Voltage
The output low voltage (V\textsubscript{OL}) is the same thing as V\textsubscript{CE(SAT)} and can be determined by, Figure 1, Figure 2, or Electrical Characteristics.

10.2.2.3 Power Dissipation & Temperature
The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use the below equation to calculate ULN2803A on-chip power dissipation P\textsubscript{D}:

\[
P_{\text{D}} = \sum_{i=1}^{N} V_{\text{OLi}} \times I_{\text{Li}}
\]

Where:
N is the number of channels active together.
V\textsubscript{OL} is the OUT\textsubscript{i} pin voltage for the load current I\textsubscript{Li}. This is the same as V\textsubscript{CE(SAT)}

(2)

In order to guarantee reliability of ULN2803A and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (P\textsubscript{D(MAX)}) dictated by below equation Equation 3.

\[
P_{\text{D(MAX)}} = \frac{(T_{J(MAX)} - T_{A})}{\theta_{JA}}
\]

Where:
T\textsubscript{J(MAX)} is the target maximum junction temperature.
T\textsubscript{A} is the operating ambient temperature.
\theta_{JA} is the package junction to ambient thermal resistance.

(3)

It is recommended to limit ULN2803A IC’s die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.
10.2.3 Application Curves

The following curves were generated with ULN2803A driving an OMRON G5NB relay – $V_{in} = 5.0\text{V}; V_{sup} = 12 \text{V}$ & $R_{COIL} = 2.8 \text{kΩ}$

![Figure 14. Output Response with Activation of Coil (Turn On)](image1)

![Figure 15. Output Response with De-activation of Coil (Turn Off)](image2)

11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803A. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

![Figure 16. Package Layout](image3)
13 Device and Documentation Support

13.1 Trademarks
All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULN2803ADW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td>Samples</td>
</tr>
<tr>
<td>ULN2803ADWG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td>Samples</td>
</tr>
<tr>
<td>ULN2803ADWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td>Samples</td>
</tr>
<tr>
<td>ULN2803ADWRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>18</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ULN2803A</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**: Orientation for sprocketing
- **User Direction of Feed**: Direction for tape feeding
- **Pocket Quadrants**: Areas for tape pockets

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>DW</td>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<th>SPQ</th>
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*www.ti.com 3-Mar-2014*
### N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

**16 PINS SHOWN**

#### NOTES:
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

#### Dimensions

<table>
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<tr>
<th>PINS **</th>
<th>14</th>
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<th>18</th>
<th>20</th>
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<td>DIM</td>
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<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
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<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
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**MS-001 VARIATION**

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<tr>
<th></th>
<th>AA</th>
<th>BB</th>
<th>AC</th>
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</table>

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**4040049/E 12/2002**

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NOTES:  
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994. 
B. This drawing is subject to change without notice. 
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15). 
D. Falls within JEDEC MS-013 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
<td>Copyright © 2015, Texas Instruments Incorporated</td>
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