UART IP CORE

Designed By - Mitu Raj

Revised on – 15th Jan 2017
UART IP core – Specifications

- 8-bit
- Programmable baud rates from 600-115200
- Start, Stop bits and No parity included
- Clock input - 100 MHz
- Maximum permissible frequency mismatch for data reception = +/- 4.0%
- Maximum error in baud rate generation = +/- 0.005%
- Tested in Artix-7 FPGA for 100 MHz clock input
**UART IP core - Interface signals**

- Load – Pulled low, to start transmission
- Reset – Active low signal to reset the module
- Enable – Active low chip enable signal
- Clock in – Input clock
- Baud rate – To set baud rate
- Tx Data in – Parallel 8 bit data input from processor
- Tx Data out – Serial data output
- Rx Data in – Serial data input
- Rx Data out – Parallel data output to processor
- Tx intr – Transmit interrupt to processor
- Rx intr – Receive interrupt to processor
- ERROR – To indicate error in data reception

**Setting baud rate**

<table>
<thead>
<tr>
<th>Baud rate vector input</th>
<th>Baud rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>600</td>
</tr>
<tr>
<td>0001</td>
<td>1200</td>
</tr>
<tr>
<td>0010</td>
<td>2400</td>
</tr>
<tr>
<td>0011</td>
<td>4800</td>
</tr>
<tr>
<td>0100</td>
<td>9600</td>
</tr>
<tr>
<td>0101</td>
<td>19200</td>
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<tr>
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<td>38400</td>
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<tr>
<td>0111</td>
<td>57600</td>
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<tr>
<td>1000</td>
<td>115200</td>
</tr>
</tbody>
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