library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

definition clocks is
    Port ( CLK : in STD_LOGIC;
          clock_480 : out STD_LOGIC;
          clock_centi : out STD_LOGIC);
end clocks;

architecture Behavioral of clocks is

signal clk1, clk2 : STD_LOGIC;

begin

clk_480hz : process (CLK) --clock runs at 480Hz to keep all the LEDs on
variable count1 : unsigned (17 downto 0):="00000000000000000000";
begin
    if (rising_edge(CLK)) then
        if count1 = "110010110111001010" then --counting to 208333
            clk1 <= not clk1;
            count1 := "00000000000000000000";
        end if;
        count1 := count1 + 1;
    end if;
end process;

clk_centi : process (CLK) --clock runs at 0.5MHz to count in centiseconds
variable count2 : unsigned (18 downto 0):="00000000000000000000";
begin
    if (rising_edge(CLK)) then
        if count2 = "111101000010010010" then --counting to 500000
            clk2 <= not clk2;
        end if;
    end if;
end process;
count2 := "0000000000000000000";
end if;
count2 := count2 + 1;
end if;
end process;

clock_480 <= clk1; --setting this clock to a signal to make input for display module
clock_centi <= clk2; --setting this clock to a signal to make input for display module

end Behavioral;